CLAIMS AMENDMENTS

1. (Original) A memory bank having words that are addressable by addresses and having multiple sections, the memory bank comprising:

a plurality of sections, each section representing a subdivision of a word of memory, each section having a row enable line for each row of the memory and a column enable line for each column of the memory for enabling access to a subdivision of a word of memory, each section having a section enable line for enabling access to that section;

for each row of each section, row enabler logic that enables the row enable line for that row of that section only when the section enable line for that section is enabled; and

for each section, column enabler logic that enables a column enable line for that section only when the section enable line for that section is enabled.

2. (Original) The memory bank of claim 1 wherein the memory bank is part of a multiport memory device and wherein the section enable lines are enabled based on the accessing port.

3. (Original) The memory bank of claim 1 wherein different rows of different sections can be simultaneously accessed to satisfy different memory access requests.

4. (Original) The memory bank of claim 1 wherein row and column address enable signals are buffered to accommodate row and column latencies.

5. (Original) The memory bank of claim 1 including configuration information storage for selectively enabling sections.

6. (Original) The memory bank of claim 5 wherein the memory bank is part of a multiport memory device and the selective enabling of sections is on a port-by-port basis.

7. (Currently amended) A memory bank having words that are addressable by addresses and having multiple sections, the memory bank comprising:

a plurality of sections, each section representing a subdivision of a word of memory, each word of memory being accessible via an address, each section being selectively enabled so that row enable lines to a section are only enabled when the subdivision of the word represented by the section is accessed wherein only a portion of a word corresponding to enabled sections is accessible so that sections that are not enabled use less power than sections that are enabled.

8. (Original) The memory bank of claim 7 wherein the address is divided into a row portion and a column portion and the memory bank includes a row decoder and a column decoder to selectively accesses a word of the memory bank.

9. (Original) The memory bank of claim 8 wherein output of the row decoder and output of the column decoder only drive sections that are enabled.

10. (Original) The memory bank of claim 9 wherein the outputs are buffered to accommodate row and column latencies.

11. (Original) The memory bank of claim 7 wherein the memory bank is part of a multiport memory device and wherein the section enable lines are enabled based on the accessing port.

12. (Original) The memory bank of claim 7 wherein different rows of different sections can be simultaneously accessed to satisfy different memory access requests.

13. (Original) The memory bank of claim 7 including configuration information storage for selectively enabling sections.

14. (Original) The memory bank of claim 13 wherein the memory bank is part of a multiport memory device and the selective enabling of sections is on a port-by-port basis.

15. (Currently Amended) A method for providing access to memory, the method comprising:

disabling a section of the memory, the memory including multiple sections that each contain a subdivision of a word so that row enable lines to the disabled section are not enabled when a word of memory is accessed;

receiving an address for a word of memory that is to be accessed; and

accessing a subdivision of the addressed word of memory, the accessed subdivision not including the subdivision of the word in the disabled section of memory so that power is preserved by disabling the section of memory when access to the entire word is not needed.

16. (Previously presented) The method of claim 15 wherein the memory is a multiport memory and the sections can be disabled on a port-by-port basis.

17. (Previously presented) The method of claim 16 wherein different subdivisions of a word can be accessed through different ports.

18. (Previously presented) The method of claim 15 wherein the disabling of a section of the memory includes setting a configurable parameter of the memory.

19. (Previously presented) The method of claim 18 wherein the setting is stored in a latch that disables the section.

20. (Currently amended) A memory having words that are addressable by addresses, the memory comprising:

a plurality of sections that each contain a subdivision of each word; and

means for selectively disabling a section so that a row enable line to the disabled section is not enabled when a word is accessed and so that accesses to the memory access a subdivision of words that does not include the subdivision of the disabled section whereby power is saved because the section is disabled.

21. (Previously presented) The memory of claim 20 including a plurality of ports and wherein the means for selectively disabling does so on a port-by-port basis.

22. (Previously presented) The memory of claim 20 wherein the means for selectively disabling includes a latch for storing an indication of whether a section is disabled.